This course is aimed at introducing the fundamental concepts and the basic tools used in the logic design of digital systems.
六、教學進度 (Syllabi)

2008/10/15  Boolean Algebra and Logic Gates - Binary Logic and Gates - Boolean Algebra
2008/10/22  Boolean Algebra and Logic Gates - Binary Logic and Gates - Boolean Algebra
2008/10/29  Gate-Level Minimization - Two-Level Circuit Optimization - Multiple-Level Circuit Optimization
2008/11/5  Gate-Level Minimization - Two-Level Circuit Optimization - Multiple-Level Circuit Optimization
2008/11/12  Team Project or Mid-term Exam
2008/11/19  Combinational Logic - Combinational Logic Design Flow - Combinational Functions and Circuits
2008/11/26  Combinational Logic - Combinational Logic Design Flow - Combinational Functions and Circuits
2008/12/3  Combinational Logic - Combinational Logic Design Flow - Combinational Functions and Circuits
2008/12/10  Combinational Logic - Combinational Logic Design Flow - Combinational Functions and Circuits
2008/12/17  Synchronous Sequential Logic - Latches and Flip-Flops - Synchronous Sequential Circuit Analysis and Design Flow - Registers and Counters
2008/12/24  Synchronous Sequential Logic - Latches and Flip-Flops - Synchronous Sequential Circuit Analysis and Design Flow - Registers and Counters
2008/12/31  Synchronous Sequential Logic - Latches and Flip-Flops - Synchronous Sequential Circuit Analysis and Design Flow - Registers and Counters
2009/1/7  Synchronous Sequential Logic - Latches and Flip-Flops - Synchronous Sequential Circuit Analysis and Design Flow - Registers and Counters
2009/1/14  Team Project or Final Exam

二、評量方式 (Evaluation)
Participation: 10%  Team Project: 30%  Mid-term Exam: 30%  Final Exam: 30%

八、講義位址 (http://)

九、教育目標

[重新查詢]